Title: Measure Op-Amp parameters and compare the result with datasheet of corresponding Op-Amp.

- Input bias current,
- Input offset current and
- Input offset voltage,
- Slew rate
- CMRR.

Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF OPERATIONAL AMPLIFIER PARAMETERS

Aim: To measure non ideal parameter of Op amp 741c

1) **DC input offset voltage**
2) **Input bias current**
3) **Input offset current**
4) **CMRR.**
5) **Slew rate**

Apparatus:

Bread board, Resistors, Capacitors, DC power supply (0-30V, 2A), DMM, connectors.
IC 741

Set up Diagram:

Input offset voltage

Input bias current

CMRR

Slew rate

THEORY:

For an ideal operational amplifier, it is assumed that the opamp responds equally well to both ac and dc input voltage .However practical opamp does not behave this way. A practical op amp has some dc voltage at the output even with both the inputs grounded. Also under ac conditions, characteristics of op amp are frequency dependent.

An ideal opamp draws no current from the source and its response is also independent of temperature. However a real opamp does not work this way. Current is taken from the source into the opamp inputs . Also two inputs respond differently to current and voltage due to mismatch in transistors. These non ideal dc characteristics add error components to dc output voltage are input bias current

1) input offset voltage
2) input offset current
3) thermal drift

1) Input offset voltage (Vio)

   Input offset voltage is the voltage that must be applied between the two input terminals of opamp to null the output. This voltage could be positive or negative . Smaller the value of Vio better the input terminals are matched.

2) Input bias current (IB) :

   Input bias current is the average of the currents that flow into the inverting and non inverting input terminals of the op amp.

3) Input offset current (Iio):

   The algebraic difference between the inverting and non inverting terminals is referred to as input offset current. As match between two input terminals is improved, the difference between the current entering into terminals become smaller that is the Iio value decreases further.

4) CMRR:

   It is the ratio of differential voltage gain (Ad) to the common mode voltage (Acm) The differential voltage gain is obtained by applying different voltages to the inverting and non inverting terminals of the opamp. The common mode voltage gain is obtained by applying same signal to both inverting and non inverting terminal of opamp. The common mode voltage gain is very low and hence the CMRR is a very high value.

5) Slew rate :

   It is the maximum rate of change of output voltage per unit of time and is expressed in volts per microseconds. Slew rate indicates how rapidly the output of an op amp can change in response to changes in the input frequency.

Procedure:

I) Input offset voltage:

1. Make the connections.
2. Apply dual power supply i.e. Vcc of + 12V to pin no. 7 and $-V_{EE}$ of -12v to pin no 4 of opamp IC.
3. Ground both inverting (pin no. 2) and non inverting inputs(pin no.3)
4. Measure output voltage Voo (output offset voltage).
5. Calculate input offset voltage Vio= (Ri/(Ri+Rf)*Voo

II) Measurement of input bias current:

1. Make the connections
2. Apply dual power supply i.e. +VCC of +12 to pin 7 and -V_{EE} of -12V to pin 4 of opamp IC
3. Short A and B measure Vo= V_{01}
4. Calculate IB1=V_{01}/1MΩ
5. Short C and D and measure VO=V_{02}
6. Calculate IB2=V_{02}/1 MΩ
7. Calculate the input bias current using formulae.
8. Also calculate input offset current using formulae.

III) Measurement of CMRR:

1. Make connections and apply dual supply.
2. Apply common input voltage of 1V, 1kHz
3. Measure output voltage as Vcm.
4. Calculate common mode gain as Acm=Vcm/Vi
5. Ground pin no. 3 and apply 1V at 1kHz to inverting input and measure Vd.
6. Calculate differential gain as Ad=Vd/Vi.
7. Calculate CMRR=20 log (Ad/Acm) in DB

IV) Measurement of slew rate :

1. Make the connections
2. Give square wave input of 2V at 10 KHz to non inverting input terminal.
3. Measure dv (on Y-axis) and dt (on X-axis) for rising edge and falling edge.
4. Calculate slew rate =dv/dt for rising and falling edge.

<u>Draw diagram for obtained slew rate waveform</u>

Calculation:

(Vio) CMRR

(Iio) Slew Rate

(IB)

Observation:

Sr.No.	Parameter	Observed value	Datasheet Value
1	Input offset voltage (Vio)		
2	Input offset current (Iio)		
3	Input Bias current (IB)		
4	CMRR		
5	Slew Rate		

Conclusion:

Title: Design, build and test integrator for given frequency f_a

Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDEY OF INTEGRATOR

Aim: Design, build and test integrator for given frequency f_a

Apparatus:

Sr. No.	Instrument	Specification
1	CRO	
2	Signal generator	
3	Power supply	
4	Experiment Kit	
5	Connector	

Set up Diagram:

Theory:

The Integrator:

A circuit in which the output voltage is integral of the input voltage waveform is the integrator or integrating amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by capacitor C_F as shown in figure.

The equation indicates that the output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant R_i,C_f. For example if input sine wave is sine wave , the output will be cosine wave; or if the input is square wave the output will be triangular wave.

When V_{IM}= 0, the integrator shown above works as an open loop amplifier. This is because the capacitor C_F acts as an open circuit (X_CF-=00) to the input offset voltage. In
Words, the input offset voltage and the part of input current charging capacitors C_F produce the error voltage at the output of integrator. Therefore in the practical integrator shown above produces the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F which limits the low frequency gain and hence minimizes the variation in the output voltage .Both the stability and the low frequency roll off problems are corrected by addition of a resistor R_F as shown in the practical integrator.

The frequency response of a practical integrator is as shown in the figure. From
Low frequency to Fa the gain is R_F/R_1 constant. However after F_a the gain decreases at the rate of 20dB/decade. In other word, between F_a and F_b the circuit acts as integrator. The gain limiting frequency F_a and F_b is given by
Fa = 50 Hz
Fb=20Fa =

The integrator is most commonly used in analog computers and analog to digital converter and Signal wave shaping circuit.

Procedure:

1. With the help of formula calculate value of R_F &R_1.
2. Make the connections as shown in the figure.
3. At F= 500Hz, apply 1vp-p sine wave and square wave and draw input output.

4. For frequency response , vary input frequency from 10Hz to 500Hz with 1VP-P Amplitude and measure V o/p and find out gain.
5. Plot frequency response of integrator.

Calculation:

Observation:

F_{IN}	V_{OUT}	GAIN	GAIN dB

Conclusion:

Title: Design, build and test three Op-Amp instrumentation amplifiers for typical application

Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF INSTRUMENTATION AMPLIFIER

Aim: To design and build and test RTD Based bridge circuit and interface with instrumentation amplifier.

Apparatus:

Sr. No.	Instrument	Specification
1	Dual power supply	
2	Multimeter	
3	Single power supply	
4	Experiment Kit	
5	Connector	

Set up Diagram:

Theory:

The figure shows a differential instrumentation amplifier using a transducer bridge resistance RT is resistance of which changes proportional with some physical quantity such as temperature, pressure, light intensity etc. R_T is the resistance of the transducer & R is the change in the resistance R_T

Procedure:

1. Design the circuit & connect it as shown in circuit diagram.
2. Initially balance the bridge of 100Ω resistor values.
3. Measure the output of instrumentation amplifier.
4. Now in arm RT vary the resistance to 110Ω , 120Ω , 130Ω, 140Ω and measure corresponding output voltage.
5. Now connect RTD lin arm RT and increase of RTD .For corresponding changes in resistance of RTD. For corresponding changes in resistance of RTD measure output voltage

Observation Table:

1) Measurement with RTD

Sr.No	Temperature	Voltage
1		
2		
3		
4		
5		
6		

Conclusion:

Title: Design, build and test precision half & full wave rectifier.
Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF PRECISION RECTIFIER

Aim: Build and test precision Half wave and full wave rectifier

Apparatus:

Sr. No	Instrument	Specification
1	CRO	
2	Signal generator	
3	Power supply	
4	Experiment kit	
5	Connectors	

Set up Diagram:

A. Precision Half Wave Rectifier

B. Precision Full Wave Rectifier

Theory:

The major limitations of rectifier circuits that can be implemented with ordinary diodes is that they cannot rectify the voltage below V_{IN} = 0.7V, the cut in voltage of the diode. A circuit that acts as a ideal diode can be designed by placing diode in the feedback loop of the op amp. This circuit is called as precision rectifier.

An inverting amplifier can be converted to ideal half wave rectifier by adding two diodes in the feedback path as shown in the figure A.

When input voltage V_{IN} is in positive half cycle, diode D_1 is reverse biased, so output voltage is zero. Diode D_2 conducts and hence prevents the op amp from going into negative saturation. This in turn helps to reduce the recovery time of op amp.

When input voltage V_{IN} is in negative half cycle, diode D_1 is forward biased, the circuit then acts like as inverter and output becomes positive.

A full wave rectifier or absolute value circuit is as shown in the figure. For positive input i.e. Vi>0, diode D_1 is on and D_2 is off. Both the op amp A_1 and A_2 act as inverter as shown in the equivalent circuit.

For negative input i.e. Vi<0 diode D_1 is off and D_2 is on. The equivalent circuit is as shown in the figure B

Let the output voltage of op amp be V.

V = -(2/3 Vin). By applying KCL at node A

The equivalent circuit of circuit is a non inverting amplifier as shown in the figure

V0 = (1+R/2R)(-2/3Vin)=vin.

Hence for Vin<0, the output is positive.

Procedure:

A. Half wave rectifier

- **a.** Make the connections
- **b.** Apply a sine wave of 1KHz, 1Vp-p and observe and draw waveform at the output
- **c.** Vary inout signal from 100mV to 1V peak to peak in steps of 100mV at 1KHz and measure output voltage
- **d.** Keep amplitude constant at 1Vp-p and vary input frequency towards higher side and observe effect on output and comment

B. Full wave rectifier

- **a.** Follow same procedure as half wave rectifier

1. Connect the circuit as per the circuit diagram.
2. Give a sinusoidal input of 1 VPP, 1 KHz from a signal generator.
3. Switch on the power supply and note down the output from CRO.

Observation Table:

Half Wave Rectifier

V_{IN}	V_{OUT}
100mV	
200mV	
300mV	
400mV	
500mV	
600mV	
700mV	
800mV	
900mV	
1V	

Full Wave Rectifier

V_{IN}	V_{OUT}
100mV	
200mV	
300mV	
400mV	
500mV	
600mV	
700mV	
800mV	
900mV	
1V	

Conclusion:

Title: Design, build and test Schmitt trigger and plot transfer characteristics.

Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY SCHMITT TRIGGER

Aim: To design and test the Schmitt trigger with and without reference voltage.

Apparatus:

Sr. No.	Instrument	Specification
1	CRO	
2	Signal generator	
3	Power supply	
4	Experiment Kit	
5	Connector	

Set up Diagram:

Symmetrical Schmitt trigger:

Asymmetrical Schmitt trigger:

Theory:

Schmitt trigger is inverting comparator with positive feedback. This circuit converts irregular shape waveform to a square wave or pulse. The circuit is also known as squaring circuit. The input voltage V_{IN} triggers (change the state of) output V_0 every time it exceeds certain voltage levels called as upper threshold (V_{UT}) and lower threshold voltage (V_{IT})

Hysteresis

These threshold voltages are obtained by using the voltage divider where, the voltage across R1 is feedback to the non inverting input terminal. The voltage across R1 is a variable references threshold voltage that depends on the value and polarity of the output voltage V_0 .

When V_0 = +Vsat, the voltage across R1 is called the upper threshold voltage, Vut. The input voltage V_I must be slightly more than Vut in order to switch from +Vsat to –Vsat . As long as Vin < Vut Vo is Vsat. Using voltage divider rule ,

$$Vut = \frac{R_2}{R_1+R_2} (+Vsat)$$

On the other hand when V0= -Vsat, the voltage across R1 is called the lower threshold voltage Vlt. The input voltage V_{in} must be slightly more negative than V_{It}

& in order to switch from –Vsat to +Vsat.As long as Vin> Vut, V0 is –Vsat. Using voltage divider rule,

$$V_{Lt} = \frac{R_2}{R_1+R_2} (-Vsat)$$

Thus if the threshold voltages Vut and Vlt are made larger than the input noise voltages, the positive feedback will eliminate the false output transition.

The comparator with positive feedback is said to exhibit Hysteresis, a dead band condition. That is, when the input of comparator exceeds, its output switches from –Vsat and reverts back to its original state, +Vsat, when input goes below VIt.

Hysteresis voltage = V_H = Vut-VIt

Calculations:

Symmetrical Schmitt trigger:

Asymmetrical Schmitt trigger:

Procedure:

I) Symmetrical Schmitt trigger:

1) Calculate the values of R1 and R2
2) Make the connections as shown in figure.
3) Depending upon UTP and LTP levels apply input signal amplitude at 1KHz frequency.
4) Observe and draw input and output simultaneously
5) Apply input signal to X plate of CRO and Output signal to Y plate of CRO and keep CRO in XY mode.
6) Observe and draw hysteresis loop.

II) Asymmetrical Schmitt trigger:

1) Calculate the values of R1 and R2 and reference voltage.
2) Repeat the same procedure as symmetrical Schmitt trigger.

Observations:

Parameter	From waveforms	Hysteresis loop
Symmetrical Schmitt trigger:		
Vut		
VIt		
Asymmetrical Schmitt trigger:		
Vut		
VIt		

Conclusion:

Title: Design, build and test PLL.
Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF PHASE LOCKED LOOP (PLL)

Aim: Build and test Phase Locked Loop (PLL)

Apparatus:

Sr. No	INSTRUMENT	SPECIFICATION
1	CRO	
2	Signal generator	
3	Power supply	
4	Experiment kit	
5	Connectors	

Set up Diagram:

Theory:

PLL stands for *'Phase-Locked Loop'* and is basically a closed loop frequency control system, which functioning is based on the phase sensitive detection of phase difference between the input and output signals of the controlled oscillator (CO).

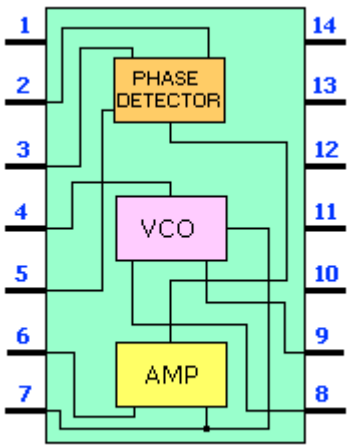


Fig. 1

The PLL is a very interesting and useful building block available as single integrated circuits from several well known manufacturers. It contains a phase detector, amplifier, and VCO, see Figure 1 and represents a blend of digital and analog techniques all in one package.

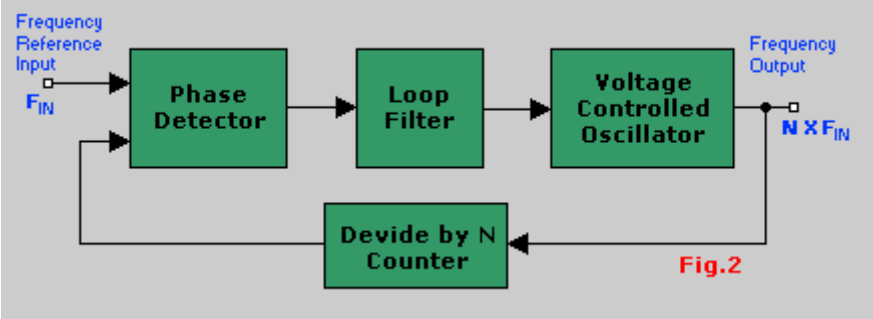
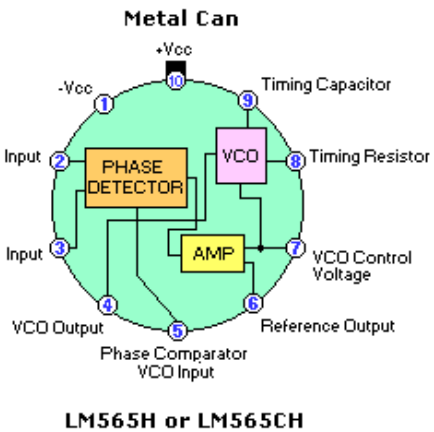
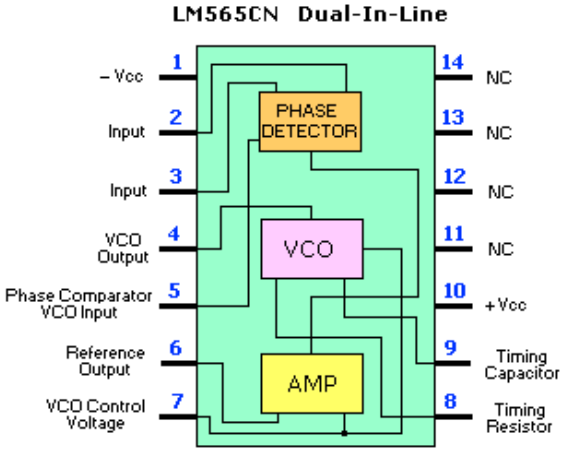


Figure 2 shows the classic configuration. The phase detector is a device that compares two input frequencies, generating an output that is a measure of their phase difference (if, for example, they differ in frequency, it gives a periodic output at the difference frequency). If f_{IN}doesn't equal f_{VCO}, the phase-error signal, after being filtered and amplified, causes the VCO frequency to deviate in the direction of f_{IN}. If conditions are right, the VCO will quickly "lock" to f_{IN} maintaining a fixed relationship with the input signal.

The LM565 is a general purpose Phase-Locked Loop IC containing a stable, highly linear voltage controlled oscillator (VCO) for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system--bandwidth, response speed, capture and pull in range may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.





A Phase-Locked Loop has basically three states:

1) Free-running

2) Capture

3) Phase-Lock

The range over which the loop system will follow changes in the input frequency is called the lock range. On the other hand, the frequency range in which the loop acquires phase-lock is the capture range, and is never greater than the lock range.

A low-pass filter is used to control the dynamic characteristics of the phase-locked loop. If the difference between the input and VCO frequencies is significantly large, the resultant signal is out of the capture range of the loop. Once the loop is phase-locked, the filter only limits the speed of the loop's ability to track changes in the input frequency. In addition, the loop filter provides a sort of short-term memory, ensuring a rapid recapture of the signal if the system is thrown out of lock by a noise transient. However, a design of a loop filter represents a compromise in that the parameters of that filter restrict the loop's capture range and speed, it would almost be impossible for the phase-locked loop to lock without it.

Obesrvation:

Free Running Frequency	
Lock Range	
Capture Range	

Conclusion:

Title: Design and implement 2bit R-2R ladder DAC
Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF 2 BIT D TO A CONVERTER

Aim: Build and test 2 bit D to A Converter using R-2R Ladder

Apparatus:

Sr. No	Instrument	Specification
1	Power supply	
2	Experiment kit	
3	Connectors	
4	Multimeter	

Set up Diagram:

Theory:

A digital to analog converter (DAC) is a device that converts digital numbers (binary) into an analog voltage or current output.

Types of DAC

1. Resistor String
2. Binary Weighted Resistor
3. R-2R Ladder

Working of 2 bit R-2R DAC:

Considering a 2 bit DAC as shown in the diagram above where b2 and b1 correspond to the binary word 0 1. The binary input can either be high (+5V) or low (0V). The circuit can be simplified in the equivalent form as shown below.

In this type of DAC the current flowing in the resistors changes as the input data changes. In the above equivalent circuit inverting input is at virtual ground (V2 = 0). The current flowing through Rth is 0.25mA for the above word. Thus current flowing through Rf is same and in turn produces output voltage as -5V.

The output voltage equation is

$$Vo = Rf(b2/2R+ b1/4R)$$

Advantages of R-2R Ladder:

a. Simplest type of DAC

b. Requires only two precision resistance value (R and 2R)

c. Easy to manufacture

d. Faster response time

Disadvantages of R-2R Ladder:

a. More confusing analysis

Observation Table:

Input		Vo (Therotical)	Vo (Practical)
b2	b1		
0	0		
0	1		
1	0		
1	1		

Conclusion:

Title: Design, build and test square & triangular wave generator.
Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF SQUARE AND TRAINGULAR WAVE GENERATOR

Aim: Design, build and test square & triangular wave generator.

Apparatus:

Sr. No	INSTRUMENT	SPECIFICATION
3	Power supply	
4	Experiment kit	
5	Connectors	

Set up Diagram:

Theory:

In the square wave generator output of opamp is forced to swing repetitively between positive saturation +Vsat and negative saturation – Vsat. The square wave generator is also called as astable multivibrator free running oscillator.

Assume that the voltage across capacitors C is zero volts at that instant the dc supply voltages $+V_{CC}$ and $-V_{EE}$ are applied. This means that the voltage V1 at the non inverting terminal is very small finite value the function of output offset voltage V_{OO} and the value of R1 and R2. Thus the differential input voltage Vid is equal to the V1 at the non inverting terminal. Even though the voltage is very small V1 will start to drive the opamp into saturation.

For example suppose that the output voltage V_{OOT} is positive and that therefore voltage V1 is positive. Since initially capacitor act as short circuit the gain of opamp is very large (A); hence V1 drives the output of opamp to its positive saturation +Vsat, which capacitor starts charging towards +V sat through resistor R. However as soon as the voltage V2 across capacitor is slightly more positive than V1 , the output of opamp is forced to switch to negative –Vsat and capacitors starts discharging.

Procedure:

1. Make the connections.
2. Observe and draw waveforms at the output and across capacitors.

3. Measure Ton and Toff.

Calculation for square wave generator:

Observation:

	Symmetric square wave generator
Ton	
Toff	

Theory:

Triangular wave can be generated using integrator circuit when square wave output is applied to its input. So triangular wave generator consists of square wave generator followed by an integrator circuit.

Circuit Diagram:

Resistor R1 and capacitor C1 determines the frequency of the square wave. Resistor R2 and R3 forms a voltage divider set up which feedback a fixed fraction of the output to the non inverting input of the IC.

Initially, when power is not applied the voltage across the capacitor C1 is 0. When the power supply is switched ON .the C1 starts charging through the resistor R1 and the output of the opamp will be high (+Vcc). A fraction of this high voltage is fed back to the non-inverting pin by the resistor network R2,R3.When the voltage across the charging capacitor is increased to apoint the voltage at the inverting pin is higher than the non-inverting pin, the output of the opamp swing to negative saturation (-Vcc). The capacitor quickly discharges through R1 and start charging in the negative direction again through R1. Now a fraction of the negative high output (-Vcc) is fed back to the non inverting pin by the feedback network

R2. When the voltage across the capacitor become so negative that the voltage at the inverting pin is less than the voltage the non inverting ,the output of the opamp swings back to the positive saturation Now the capacitors through R1 and starts charging in positive direction. This cycle is repeated over time and the result is a square wave swinging between +Vcc and –Vcc at the output of opamp.

If the values of R2 and R3 are made equal, Then the frequency of the square wave can be expressed using the following equation.

$$F=1/(2.1976R1C1).$$

Integrator:

Next part of the triangular wave generator is the opamp integrator. Instead of using a simple passive RC integrator an active integrator based on opamp is used here. The opamp IC used in this stage is also Ua 741(IC2). Resistor R5 along with R4 sets the gain of the integrator and resistor R5 along with C2 sets the bandwidth. The square wave signal is applied to the inverting input of the opamp through the input resistor R4. The opamp integrator part of the circuit is shown in the fig. Below.

Observation:

Plot square wave and triangular wave signal.

Conclusion:

Title: Design and implement V-I converter
Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF V to I CONVERTER

Aim: Design and implement V-I converter

Apparatus:

Sr. No	Instrument	Specification
1	Power supply	
2	Experiment kit	
3	Connectors	
4	Multimeter	

Set Up diagram:

Theory:

A voltage to current converter accepts the input in the voltage form (Vi) & produces output in the form of current (I_0).The output current is proportional to input voltage.

$$I_0 = A\ Vi$$

Where A is called as the sensitivity of V to I converter, in Ampere per volt .The voltage to current (V to I) converters can be classified into two categories, depending on the position of the load.

They are: V to I converter with floating load and V to I converter with grounded load

1. Voltage to current converter with floating load:

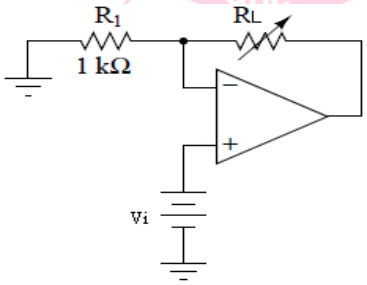


Fig: Voltage to current converter with floating load

Figure shows a voltage to current converter with floating load. This load (RL) is called as floating load because it is not connected to ground.

Operation:

The input voltage is applied to the non inverting (+) terminal of the OP-AMP. Load resistance RL is connected in place of the feedback resister RF (in the conventional non inverting amplifier).

This circuit is also called as current series negative feedback amplifier. This is because the feedback voltage across R1 is proportional to the output current Io & appears in series with the input voltage.

$$I_O = Vin/R_1$$

Sensitivity of this circuit is (1/R1). Hence sensitivity can be increased by decreasing the value of R1. Voltage to current converter is used in applications such as low voltage dc &ac voltmeters, LED & zener diode testers etc.

Observation Table:

Voltage to current converter with floating load for vin in the range from 1V to 5 V

Sr.No.	Vin	I theoretical	I practical

Conclusion:

Title: Design, build and test Wein Bridge Oscillator
Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF WEIN BRIDGE OSCILLATOR

Aim:- To study the wein bridge oscillator.

Apparatus:-

Sr.NO	INSTRUMENT	SPECIFICATION
1	CRO	
2	Power supply	
3	Experiment kit	
4	Connector	

Set Diagram:

Theory:-

Because of its simplicity and stability, one of the most commonly used audio frequency oscillator is the Wein Bridge. The wein bridge oscillators in which the wein bridge circuit is connected between the amplifier input terminals and output terminal. The bridge has series RC network in one arm and a parallel RC network in the adjoining arm. In the remaining two arms of bridge , resistor R1 and RF are connected.

The Phase angle criterion for oscillation is that total phase shift around the circuit must be 0. This condition occurs when bridge is balanced, that is at resonance .Frequency of oscillation is exactly the resonance frequency and is given by

$$Fa=1/(2\prod RC)$$

At this frequency , the gain required for sustained oscillation is

$$Av=1/\beta=3$$

$$1+RF/R1=3$$

$$Rf=2R1.$$

Calculation:

Procedure:

1. Connect the components as shown in the circuit diagram.
2. Switch on the power supply and CRO.
3. Note down the output voltage at CRO.
4. Plot the output waveform on the graph.

Observation:

Peak to peak amplitude of output = volts.

Frequency of oscillation = Hz

Conclusion:

Title: Study of Sample and Hold Circuit
Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF SAMPLE AND HOLD CIRCUIT

Aim: Build and test sample and hold circuit.

Apparatus:

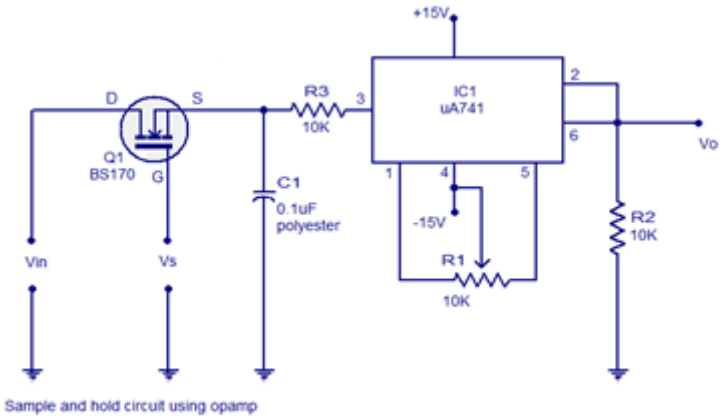
Sr. No	Instrument	Specification
1	CRO	
2	Signal generator	
3	Power supply	
4	Experiment kit	
5	Connectors	

Set up Diagram:

Theory:

As the name indicates, a sample and hold circuit is a circuit which samples an input signal and holds onto its last sampled value until the input is sampled again

A/D circuits require the input signal to remain constant during the conversion process; however, real world signals may fluctuate rapidly. The Sample and Hold (S/H) is a device that makes its output follow the input until it is told to hold this value. It then maintains the output as steady as possible, regardless of fluctuations of the input, until released to follow the input again.



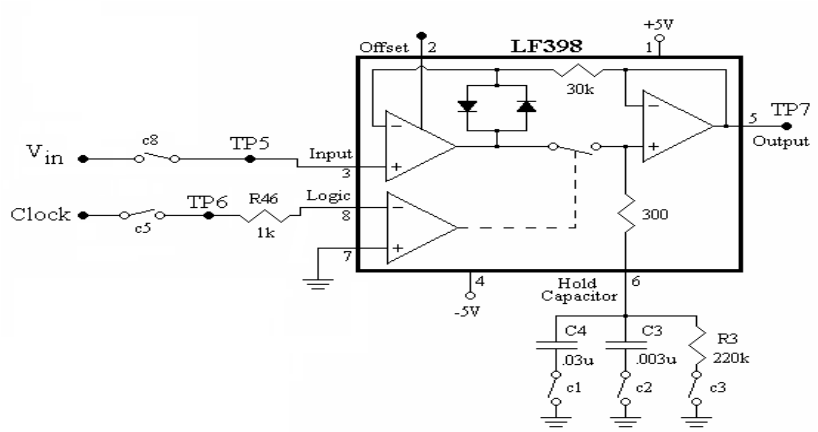
Sample and hold circuit using opamp

The signal to be sampled (Vin) is applied to the drain of MOSFET while the sample and hold control voltage (Vs) is applied to the source of the MOSFET. The source pin of the MOSFET

is connected to the non inverting input of the op-amp through the resistor R3. C1 which is a polyester capacitor serves as the charge storing device. Resistor R2 serves as the load resistor while preset R1 is used for adjusting the offset voltage.

During the positive half cycle of the Vs, the MOSFET is ON which acts like a closed switch and the capacitor C1 is charged by the Vin and the same voltage (Vin) appears at the output of the op-amp. When Vs is zero MOSFET is switched off and the only discharge path for C1 is through the inverting input of the op-amp. Since the input impedance of the op-amp is too high the voltage Vin is retained and it appears at the output of the op-amp.

The time periods of the Vs during which the voltage across the capacitor (Vc) is equal to Vin are called sample periods (Ts) and the time periods of Vs during which the voltage across the capacitor C1 (Vc) is held constant are called hold periods (Th). Taking a close look at the input and output wave forms of the circuit will make it easier to understand the working of the circuit.



The LF398 is a basic and common S/H monolithic IC. It consists of an input and output buffer amplifiers, and a digital switch. The hold capacitor is connected externally. During the sample mode, the charge on the capacitor follows the analog input signal. In the hold mode, the input amplifier is disconnected and the capacitor holds the charge. The capacitor is discharged by the follower amplifier.

Obesrvation:

Plot waveform of original signal, sample and hold signal

Conclusion:

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Title: Study of 2 bit Flash ADC
Experiment No. _____

Roll No.: _____ Name: _____

Date of performance: _____

Date of Submission: _____

Grade: _____

Signature:

STUDY OF 2 BIT FLASH TYPE ADC

Aim: Build and test 2 bit Flash type ADC

Apparatus:

Sr. No	Instrument	Specification
1	Power supply	
2	Experiment kit	
3	Connectors	

Set up Diagram:

Theory:

The process of converting an analog voltage into an equivalent digital signal is known as Analog to Digital Conversion, abbreviated as ADC. An ADC is an electronic circuit which converts its analog input to corresponding binary value. The output depends up on the coding scheme followed in the ADC circuit. For example Analog value may convert to Gray code, excess 3 code and so on.

Analog to Digital converter ICs are also available to do this operation. Which reduce the circuit complexity such that a single IC capable of doing Analog to Digital Conversion.

The circuit below shows a 2 bit ADC circuit using LM324 comparator IC. A potential divider network and some combinational circuits are used for making this simple ADC.

LM324 best suited for Analog to Digital Converters because it has four embedded op amps, it require Vcc (5V) and ground only. No need of -Vcc like 741 op amp.

Components Required for ADC

Resistors (1Kx4)

IC LM324

IC 7404

IC 7432

IC 7409

This is a simultaneous ADC, Simultaneous ADC is also called flash ADC and the speed of conversion is very fast. Reference voltage i.e Vref of 5 volts is applied to the comparators. Comparators continuously compare reference voltage at inverting terminal and analog voltage at non inverting terminal.The reference voltage of each comparator is derived from potential divider network.

- Reference voltage of lower comparator : Vref (1/4) = Vref /4
- Reference voltage of middle comparator : Vref (2/4) = Vref /2
- Reference voltage of upper comparator : Vref (3/4)

If the analog input exceeds the reference voltage to any comparator, that comparator turns ON.If all the comparators are OFF, the analog input signal will be between 0 and Vref /4.

When lower comparator ON and others are OFF, then input must be between Vref /4 and Vref /2.For input voltage between Vref /2 and Vref (3/4) , Lower and middle comparators are ON.Above Vref (3/4), all the three comparators will ON.Thus the input analog voltage get converted in to encoded form with 3 output bits, but actually we need binary output like 00, 01, 10, and 11.To represent 4 states in binary, only 2 bits are needed, so we are using a digital combinational code converter circuit with 3 logic gates. Thus it is possible to get binary outputs like 00, 01, 10, and 11.

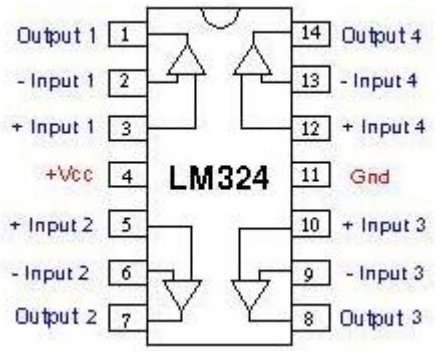
Truth Table of 2 bit Flash ADC:

Analog Input	**Comparator Output**			**Binary Output**	
	A	**B**	**C**	**X**	**Y**
0 to 1/4 Vref	0	0	0	0	0
1/4 Vref to 2/4 Vref	0	0	1	0	1
2/4 Vref to 3/4 Vref	0	1	1	1	0
3/4 Vref to Vref	1	1	1	1	1

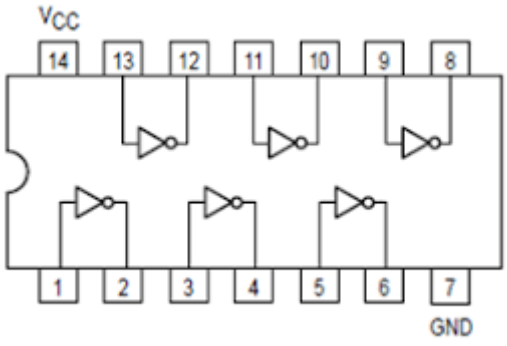
Design of Combinational Circuit (using K-map):

IC pin out:

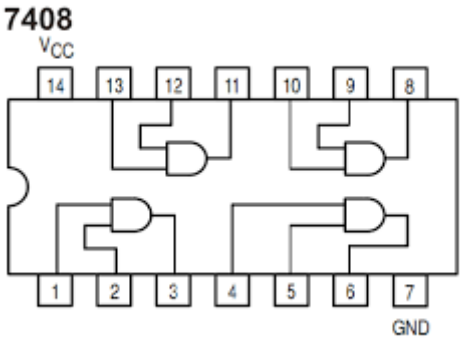
IC LM324



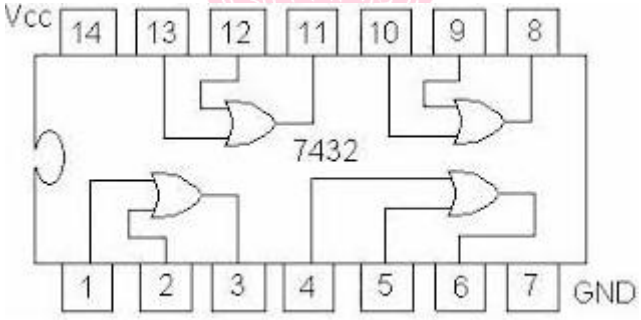
IC 7404 (NOT GATE)



IC 7408 (AND GATE)



IC 7432 (OR GATE)



Conclusion: